CLAIMS

1. A processor comprising:

a plurality of pipelines, each pipeline having a plurality of pipeline stages for executing an instruction on successive clock cycles; and

stall control circuitry which controls the stalling of instructions in the pipelines in response to a stall signal generated in any one of the pipelines;

wherein the stall control circuitry is adapted to stall the execution of an instruction in a pipeline not generating the stall signal at least one clock cycle later than the execution of an instruction in a pipeline generating the stall signal, and to release the stall in the pipeline not generating the stall signal at least one clock cycle later than the stall in the pipeline generating the stall signal.

2. A processor according to claim 1 wherein the stall control circuitry is arranged such that, when a pipeline stage in a first pipeline receives a stall signal from a second pipeline, the execution of instructions in the pipeline stage in the first pipeline is not stalled if that pipeline stage stalled in the previous cycle in response to a stall signal generated by the first pipeline.

3. A processor according to claim 1 wherein the stall control circuitry is arranged such that, when a pipeline generates a stall signal at a stage i, all stages up to and including stage i of that pipeline are stalled.

4. A processor according to claim 1 wherein, when a pipeline generates a stall signal at a stage i, all stages up to and including stage i of that pipeline

are stalled on a given clock cycle, and all stages up to and including stage i+m of a pipeline not generating a stall signal are stalled m clock cycles later than said given clock cycle, where m is an integer greater than or equal to 1.

5. A processor according to claim 1 wherein the processor comprises a plurality of pipeline clusters, each cluster comprising a plurality of pipelines.

6. A processor according to claim 5 wherein the stall control circuitry is arranged to stall execution of instructions in pipelines within a cluster in the same clock cycle.

7. A processor according to claim 5 wherein the stall control circuitry is arranged to stall the execution of instructions in pipelines in a cluster not generating the stall signal at least one clock cycle later than the execution of instructions in pipelines in a cluster generating the stall signal.

8. A processor according to claim 1 wherein, in operation, instructions entering the respective pipelines in parallel exit the pipelines in parallel.

9. A processor according to claim 1 wherein, in operation, different instructions are executed in different pipelines.

10 A processor according to claim 1, being a VLIW processor in which instructions from a VLIW instruction packet are issued in parallel to the pipelines.

11. A processor according to claim 1 wherein each

pipeline includes at least one execute stage in which an instruction is at least partially executed.

12. A processor according to claim 1 wherein the pipelines are not flushed in response to the stall signal.

13. A processor according to claim 1 wherein the stall control circuitry is distributed between two or more pipeline stages.

14. A processor according to claim 1 wherein two or more pipeline stages each have associated stall control circuitry for controlling the stalling of that pipeline stage.

15. A processor according to claim 14 wherein the stall control circuitry in each pipeline stage is arranged to generate a global stall signal for stalling another pipeline, and to receive a global stall signal from another pipeline for stalling the pipeline stage with which the circuitry is associated.

16. A processor according to claim 15 wherein the stall control circuitry does not generate a global stall signal if the associated pipeline stage is subject to a global stall from the same stage or later in another pipeline.

17. A processor according to claim 14 wherein the stall control circuitry in each of the two or more pipelines is substantially the same.

18. A processor according to claim 1 wherein a pipeline stage is not stalled if there is a bubble in that pipeline stage.

19. A processor comprising a plurality of pipelines, each pipeline having a plurality of pipeline stages which carry out a series of operations on information passing through the pipelines, two or more pipeline stages each being provided with associated stall control circuitry which control the stalling of that pipeline stage, the control circuitry comprising:

a circuit portion which generates a hold signal for stalling the associated pipeline stage in response to either a local stall signal generated by that pipeline stage or a global stall signal generated by another pipeline;

a circuit portion which generates a global stall signal for stalling another pipeline in response to said local stall signal; and

a circuit portion which delays the global stall signal such that the global stall signal is asserted a given number of clock cycles later than the hold signal is asserted, and the global stall signal is released the same number of clock cycles later than the hold signal is released.

20. A processor comprising a plurality of pipelines, each pipeline having a plurality of pipeline stages for carrying out a series of operations on information passing through the pipelines, two or more pipeline stages each being provided with associated stall control circuitry for controlling the stalling of that pipeline stage, the control circuitry comprising:

means for generating a hold signal for stalling the associated pipeline stage in response to either a local stall signal generated by that pipeline stage or a global stall signal generated by another pipeline;

means for generating a global stall signal for stalling another pipeline in response to said local stall signal; and

means for delaying the global stall signal such that the global stall signal is asserted a given number of clock cycles later than the hold signal is asserted, and the global stall signal is released the same number of clock cycles later than the hold signal is released.

21. A processor comprising:

a plurality of pipelines, each pipeline having a plurality of pipeline stages for executing an instruction on successive clock cycles; and

stalling means for stalling the execution of instructions in all of the pipelines in response to a stall signal generated in any one of the pipelines;

wherein the stalling means is adapted to stall the execution of an instruction in a pipeline not generating the stall signal at least one clock cycle later than the execution of an instruction in a pipeline generating the stall signal, and to release the stall in the pipeline not generating the stall signal at least one clock cycle later than the stall in the pipeline generating the stall signal.

22. A method of operating a processor, the processor comprising a plurality of pipelines, each pipeline having a plurality of pipeline stages for executing instructions on successive clock cycles, each pipeline being capable of generating a stall signal, the method comprising:

generating a stall signal in one of the pipelines;

stalling the execution of an instruction in the pipeline generating the stall signal;

stalling the execution of an instruction in a pipeline not generating the stall signal at least one clock cycle later;

releasing the stall in the pipeline generating the stall signal; and

releasing the stall in the pipeline not generating the stall signal at least one clock cycle later.